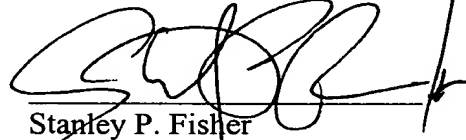


In view of the above amendments and Applicant's comments stated herein, Applicant respectfully requests an early and favorable action on the merits.

Respectfully submitted,



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Marked Up Version of the Claims

5. A level conversion circuit according to Claims 1 ~~or 4~~, wherein a high resistance element for pull-up use and a high resistance element for pull-down use are connected respectively in parallel to said first p-channel type MOS transistor and said second n-channel type MOS transistor.
6. A level conversion circuit according to Claims 1 ~~or 5~~, wherein the ratio between the gate width and the gate length of said first p-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said second p-channel type MOS transistor, and the ratio between the gate width and the gate length of said second n-channel type MOS transistor is set to be greater than the ratio between the gate width and the gate length of said first n-channel type MOS transistor.